EE 500 GRADUATE COLLOQUIUM

Spring 2014

You are cordially invited to

"Characterization of BTI Induced Variability in Scaled Metal Gate / High-K CMOS Technologies"

By

Dr. Andreas Kerber

GLOBALFOUNDRIES

Technology Reliability Development

Date: March 27, 2014

Time: 4:00 pm

Location: 160 Willard Bldg.

Abstract

Time-zero and time dependent variability is a growing concern for aggressively scaled transistor technologies with metal gate/high-k stacks. Bias temperature instability (BTI) in PMOS as well as NMOS devices is considered the most dominant time dependent variability component and needs to be modeled using stochastic processes. The physical nature of the stochastic process is still under debate and to support the model development efforts large statistical data sets are essential. In this presentation, we will focus on the characterization challenges related to stochastic BTI process in small area CMOS devices and discuss the large scale data we collected on discrete SRAM and logic devices. Finally we will elaborate on the impact of BTI induced variability on End-of-Life threshold voltage distributions and show that BTI induced variability is not the major contributing factor in the post stress threshold voltage variability in planar metal gate/high-k CMOS devices.

Biography

Andreas Kerber was born in Schnann, Austria, and received his Diploma in physics from the University of Innsbruck, Austria, in 2001, during which time he was working at Bell Laboratories, Lucent Technologies (Murray Hill, NJ, USA) on the electrical characterization of ultra-thin gate oxides. In 2001, he joined Infineon Technologies in Munich, Germany. From 2001 to 2003, he was assigned to International SEMATECH at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. At the same time he fulfilled the requirements for a PhD in electrical engineering and defended his thesis at the TU-Darmstadt, Germany, with honors. From 2004 to 2006, he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany, responsible for the dielectric reliability qualification of process technology transfers of 110 and 90 nm memory products. At the same time he developed a fast wafer-level data acquisition setup for time-dependent dielectric breakdown (TDDB) testing with sub-ms time resolution. In 2006, he joined AMD in Yorktown Heights, NY, and now is with

GLOBALFOUNDRIES in Malta, NY, working as a Senior Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation. Dr. Kerber has contributed to more than 80 journal and conference publications and presented his work at international conferences, including the VLSI Technology Symposium, the International Electron Device Meeting (IEDM) and the International Reliability Physics Symposium (IRPS). In addition, he has presented invited talks at the Workshop of Dielectrics in Microelectronics (WoDIM), the Semiconductor Interface Specialist Conference (SISC) and given tutorials on metal gate / high-k reliability characterization at the International Integrated Reliability Workshop (IIRW) and IRPS. Dr. Kerber has served as a technical program committee member for the SISC (2006, 2007), IRPS (2007, 2011, 2012, 2014), IEDM (2011, 2012), Infos (2013) and is a Senior Member of the IEEE.