SUMEET KUMAR GUPTA

Joseph R. and Janice M. Monkowski Assistant Professor of Electrical Engineering
The Pennsylvania State University
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CONTACT

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RESEARCH INTERESTS

- Nano-electronics and Spintronics
- Device-Circuit-Architecture Co-design in CMOS and Post-CMOS Technologies
- Low power Variation Aware VLSI Circuit Design
- Nano-scale Device Modeling and Simulations

EDUCATION

- Ph.D. – *Purdue University, W. Lafayette* *Aug 2008 to Oct 2012*
  G.P.A.: 4.0/4.0
  Thesis: Technology-Circuit Co-design and Analysis of Nano-scale Multi-Gate FETs for Memory Applications
  Advisor: Prof. Kaushik Roy
- M.S. in Electrical and Computer Engineering - *Purdue University, W. Lafayette*
  Specialization in VLSI Design and Semiconductor Devices *Aug 2006 to Aug 2008*
  G.P.A.: 4.0/4.0
  Thesis: Modeling and Analysis of Digital Computation in Ultra-subthreshold Regime: Approaching CMOS Limits.
  Advisor: Prof. Kaushik Roy
- B. Tech. in Electrical Engineering - *IIT Delhi* *Aug 2002 to May 2006*
  G.P.A.: 9.473/10
  Thesis: Design of Low Power High Performance Superscalar Microprocessor Core.
  Advisors: Prof. G. S. Visweswaran and Prof. P. R. Panda

ACADEMIC AWARDS AND ACHIEVEMENTS

- **DARPA Young Faculty Award** 2016
- **Monkowski Career Development Professorship in EE** 2014
- **6th TSMC Outstanding Student Research Bronze Award.** 2012
- **Intel Ph.D. Fellowship.** *2009 to 2010*
- **Certificate of Recognition for outstanding job** during Summer Internship by Intel Labs. *2010*
- **Outstanding Teaching Assistant Award** by the Office of Provost, Purdue University. *2007*
- **Magoon Award for exceptional service as a teaching assistant** by the School of Electrical and Computer Engineering, Purdue University. *2007***.**
- Certificates of merit for excellent academic performance **(top 7% in the batch**) in the first, second, sixth and seventh semesters at IIT Delhi. *2002 to 2006*
- National Talent Search Examination (NTSE) Scholarship. *2000*

WORK EXPERIENCE

Assistant Professor of Electrical Engineering, Penn State University

Jan 2014 – Present

Senior Engineer at Qualcomm Inc. *October 2012 – Jan 2014*

- Standard cell library development for deeply scaled technologies.
- Benchmarking methodologies for standard cells.

Research Assistant at Nanoelectronics Research Lab, Purdue University

Aug 2008 to Oct 2012

- Worked with Prof. Kaushik Roy in the areas of low power digital circuit design and modeling and analysis of semiconductor devices.

Summer Intern at Intel Corporation *May 2010 to Sept 2010*

- Core-to-core variation measurement and characterization of a 48 core processor in terms of maximum core frequency, L2 cache minimum voltage, leakage current and dynamic capacitance for applications like Linpack, Stencil and NASA benchmarks.
- Developed a look-up table based model for the chip power, based on the measurements.

Graduate Instructor at Purdue University *June 2008 to Aug 2008*

- Taught *"Linear Circuit Analysis" (ECE 202)* to a class of sophomore level students.
- Responsibilities included designing the course, delivering lectures, setting and grading exams and homework assignments and managing the whole course.

Co-Op at Advanced Micro Devices Inc. *Jan 2008 to May 2008*

- Circuit implementation and analysis, including logic equivalency check (LEC), cell placement, timing analysis, block merge.
- Characterized a tool that automatically sized the clock gating logic.
- Developed PERL scripts to perform stability, write-ability and weak bit analysis of state elements under process variations.

Teaching Assistant at Purdue University *Aug 2006 to Dec 2007*

- Assisted in teaching a sophomore level course in "*Introduction to Electronic Analysis and Design" (ECE 255)*.
- In-charge of holding regular office hours and help sessions for the students, managing course website, grading homework and exams, proctoring exams and taking lectures whenever required.

Summer Intern at National Semiconductor *May 2005 to July 2005*

- Analyzed error detecting/correcting codes for RFID tags.
- Implemented digital components of the RFID tag and their testbenches in Verilog and Specman 'e'. Simulated a complete command from reader to tag and its response back to the reader.

STUDENT ADVISEES

Ph.D. Students

- Ahmedullah Aziz: Current student
- Sumitha George (co-advised with Prof. Vijay Narayanan): Current student
- Sang-Ho Lee: Current student
- Atanu K. Saha: Current student
- Nicholas Jao (co-advised by Prof. Vijay Narayanan): Current student

Masters' Students

- Danni Wang: Graduated in May 2016, Currently at General Electric, China.
- Komala Madineedi (co-advised with Prof. Vijay Narayanan): Graduated in August 2016.
- Shreya Gupta: Current student
- Sandeep Thirumalla: Current student

- Baihua Xie: Current student
- Niharika Thakuria: Current student
- Sarbashis Das: Current student
- Anupriya Chakraborty: Current student

Undergraduate Students

- William Cane Wissing (REU Scholar): Graduated in December 2015, Currently at Intel.
- Kyle Sibert (Schreyers' Scholar): Graduated in December 2015. Currently at Northrup Grumman.
- Mark Steiner (Schreyers' Scholar): Graduated in May 2016. Currently at PowerEx Inc.
- Nicholas Jao: Graduated in May 2016. Currently in my research group as a Ph.D. student.
- Zhesheng Chen: Current student.
- Jacob Andrew Covey: Current student.

RESEARCH GRANTS AND CONTRACTS

- Semiconductor Research Corporation/DARPA – STARnet/LEAST: Co-PI with Suman Datta and Suptratik Guha, "Orbital Ordering Driven Threshold Switches for Select Devices in 3D X-Point Memories", 12/1/2015-10/30/2017. (S. K. Gupta's share: $150,000)
- Semiconductor Research Corporation – Global Research Collaboration: Co-PI with Suman Datta, "Ferroelectric Field Effect Transistor with Steep Switching Slope and Non-Volatile Functionality", 1/1/16 – 12/31/18. (S. K. Gupta's share: $75,000)
- DARPA – Young Investigator Award: PI "Ultra-Low Power Non-Volatile Processors Enabled by Ferroelectric Transistors", 9/15/2016-9/14/2019 ($785,577)
- National Science Foundation/Semiconductor Research Corporation - E2CDA: Co-PI with Saptarishi Das and Jack Sampson, "E2CDA: Type II: 2D Electrostrictive FETs for Ultra-Low Power Circuits and Architectures", 10/01/2016-09/30/2019 (S.K. Gupta's Share: $136,000)

PUBLICATIONS (* indicates S. K. Gupta's student)

Journal Articles (in chronological order)

1) A. Aziz*, N. Shukla, S. Datta and **S. K. Gupta**, "Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-design Perspective: Part I", Accepted in *IEEE Trans. on Electron Devices.*

2) A. Aziz*, N. Shukla, S. Datta and **S. K. Gupta**, "Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-

design Perspective: Part II", Accepted in *IEEE Trans. on Electron Devices.*

3) A. Aziz*, N. Jao*, S. Datta and **S. K. Gupta**, "Analysis of Functional Oxide based Selectors for Cross-Point Memories", Accepted in *IEEE Transactions on Circuits and Systems – I.*

4) S. Srinivasa, A. Aziz*, N. Shukla, X. Li, J. Sampson, S. Datta, J. P. Kulkarni, V. Narayanan and **S. K. Gupta**, "Correlated Material Enhanced SRAMs with Robust Low Power Operation", Accepted in *IEEE Trans. on Electron Devices.*

5) A. Aziz*, S. Ghosh, S. Datta and **S. K. Gupta**, "Physics-Based Circuit-Compatible SPICE Model for Ferroelectric Transistors", *IEEE Electron Device Letters*, vol. 37, no. 6, June 2016, pp: 805-808.

6) M. S. Kim, W C- Wissing*, X. Li, J. Sampson, S. Datta, **S. K. Gupta** and V. Narayanan, "Comparative Area and Parasitics Analysis in FinFET and Hetero-junction Vertical TFET Standard Cells", *ACM Journal of Emerging Technologies in Computing*, vol. 12, no. 4, July 2016, pp: 38.1-38:23.

7) A. Aziz* and **S. K. Gupta,** "Hybrid Multiplexing (HYM) for Read- and Area-Optimized MRAMs with Separate Read-Write Paths," *IEEE Transactions on Nanotechnology*, vol. 15, no. 3, pp. 473-483, May 2016.

8) N. Shukla, A. V. Thathachary, A. Agrawal, H. Paik, A. Aziz*, D. G. Schlom, **S. K. Gupta**, R. E. Herbert and S. Datta, "A steep slope transistor based on abrupt electronic phase transition", *Nature Communications,* vol. 6, no. 7812, 2015.

9) W. S. Cho, **S. K. Gupta** and K. Roy, "Device-Circuit Analysis of Double-Gate MOSFETs and Schottky-Barrier FETs: A Comparison Study for Sub-10nm Technologies", *IEEE Transactions on Electron Devices*, vol. 61, no. 12, Dec 2014.

10) S. H. Choday, **S. K. Gupta** and K. Roy, "Write-Optimized STT-MRAM Bit-cells Using Asymmetrically Doped Transistors", *IEEE Electron Device Letters*, vol. 35, no. 11, Nov 2014.

11) **S. K. Gupta** and K. Roy, "Device-Circuit Co-optimization for Robust Design of FinFET-based SRAMs ", *IEEE Design & Test of Computers*, vol. 30, no. 6, Dec. 2013 (Invited).

12) **S. K. Gupta**, J. P Kulkarni and K. Roy, "Tri-Mode Independent Gate FinFET-based SRAM with Pass-Gate Feedback: A Device-Circuit Co-design Approach for Enhanced Cell Stability", *IEEE Transactions on Electron Devices*, vol. 60, no. 11, Nov. 2013.

13) N. N. Mojumder, X. Fong, C. Augustine, **S. K. Gupta**, S. H. Choday and K. Roy, "Spin-Transfer Torque MRAMs for Low Power Applications", *ACM Journal of*

Emerging Technologies in Computing, vol. 9, no. 2, Sept. 2013.

14) **S. K. Gupta**, J. P Kulkarni, S. Datta and K. Roy, "Heterojunction Intra-band Tunneling (HIBT) FETs for Low Voltage SRAMs", *IEEE Transactions on Electron Devices,* vol. 59, no.12, Dec. 2012.

15) **S. K. Gupta**, G. Panagopoulos and K. Roy, "NBTI in n-type SOI access FinFETs in 6T SRAM and its impact on cell stability and performance", *IEEE Transactions on Electron Devices,* vol. 59, no. 10, Oct. 2012.

16) M. Sharad, **S. K. Gupta**, S. Raghunathan, P. Irazoqui and K. Roy, " Low-Power Architecture for Epileptic Seizure Detection Based on Reduced Complexity DWT", *ACM Journal on Emerging Technologies in Computing Systems*, vol. 8, no. 2, June 2012.

17) F. Moradi, **S. K. Gupta,** G. Panagopoulos, H. Mahmoodi, D. T. Wisland and K. Roy, "Asymmetrically-doped (AD) FinFET for Low Power Robust SRAMs", *IEEE Transactions on Electron Devices*, vol. 58, no. 12, December 2011.

18) **S. K. Gupta**, S. P. Park and K. Roy, "Tri-mode Independent Gate FinFETs for Dynamic Voltage/Frequency Scalable 6T SRAMs", *IEEE Transactions on Electron Devices,* vol. 58, no. 11, November 2011.

19) S. Raghunathan, **S. K. Gupta**, H. Markandeya, P.P. Irazoqui and K. Roy, "Ultra-Low-Power Algorithm design for Implantable Devices- Application to Epilepsy Prostheses", *Journal of Low Power Electronics and Applications*, vol. 1, no. 1, May 2011 (Invited).

20) N. N. Mojumder, **S. K. Gupta**, S. H. Choday, D. E. Nikonov and K. Roy, "Three-Terminal Dual-Pillar STT-MRAM Device for High-Performance Robust Memory Applications," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, May 2011.

21) A. Goel, **S. K. Gupta** and K. Roy, "Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low Power and Robust SRAMs", *IEEE Transactions on Electron Devices*, vol. 58, no. 2, Feb 2011.

22) S. Raghunathan, **S. K. Gupta**, H. Markandeya, K. Roy and P. P. Irazoqui, "A hardware-algorithm co-design approach to optimize seizure detection algorithms for implantable applications", *Journal of Neuroscience Methods*, vol 193, no. 1, Oct. 2010.

23) **S. K. Gupta**, A. Raychowdhury and K. Roy, "Digital computation in sub-threshold regime for ultra-low power operation: A device-circuit-architecture co-design perspective", *Proceedings of the IEEE,* vol. 98, no. 2, Feb 2010 (Invited).

24) S. Raghunathan, **S. K. Gupta**, M. P. Ward, R. M Worth, K. Roy and P. Irazoqui, "The design and hardware implementation of a low-power real-time seizure detection algorithm", *Journal of Neural Engineering*, vol. 6, 056005, Oct. 2009.

25) **S. K. Gupta**, A. Raychowdhury and K. Roy, "Compact models considering

incomplete voltage swing in CMOS circuits at ultra-low voltages: A circuit perspective on limits of switching energy", *Journal of Applied Physics*, vol. 105, no. 9, 094901, May 2009.

26) M. J. Kumar, V. Venkataraman and **S. K. Gupta**, "A New Grounded Lamination Gate (GLG) for Diminished Fringe Capacitance Effects in High-K Gate Dielectric MOSFETs", *IEEE Transactions on Electron Devices*, vol. 53, no. 10, October 2006.

27) M. J. Kumar, **S. K. Gupta** and V. Venkataraman, "Compact Modeling of the Effects of Parasitic Internal Fringe Capacitance on the Threshold Voltage of High-K Gate Dielectric Nanoscale SOI MOSFETs", *IEEE Transactions on Electron Devices,* vol. 53, no. 4, April 2006.

28) V. Venkataraman, **S. K. Gupta** and M. J. Kumar, "On the Parasitic Gate Capacitance of Small Geometry MOSFETs," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, July 2005.

Under Review

29) X. Li, S. George, K. Ma, W-Y Tsai, A. Aziz, J. Sampson, **S. K. Gupta**, M.-F. Chang, Y. Liu, S. Datta and V. Narayanan, "Advancing Nonvolatile Computing with Nonvolatile NCFET Latches and Flip-Flops", Under review in *IEEE Trans. on Circuits and Systems -I.*

Conference Proceedings (in chronological order)

30) **S. K. Gupta**, D. Wang, S. George, A. Aziz, X. Li, S. Datta and V. Narayanan, "Harnessing Ferroelectrics for Non-volatile Memories and Logic", to appear in *International Symposium on Quality Electronic Design,* 2017. *(Invited)*

31) N. Shukla, B. Grisafe, R. K. Ghosh, N. Jao*, A. Aziz*, J. Froujier, M. Jerry, S. Sonde, S. Rouvimov, T. Orlova, S. Guha, **S. K. Gupta**, and S. Datta, "Ag/HfO2 based Threshold Switch with Extreme Non-Linearity for Unipolar Cross-Point Memory and Steep-slope Phase-FETs", Accepted in *International Electron Device Meetings,* 2016.

32) X. Yin, A. Aziz*, J. Nahas, S. Datta, **S. K. Gupta**, M. Nimier and X. S. Hu, "Exploiting Ferroelectric FETs for Low-Power Non-Volatile Logic-in-Memory Circuits", *International Conference On Computer Aided Design*, 2016.

33) D. Wang*, S. George*, A. Aziz*, S. Datta, V. Narayanan and **S. K. Gupta**, "Ferroelectric Transistor based Non-Volatile Flip-Flop", *International Symposium on Low Power Electronics and Design (ISLPED)* 2016.

34) S. George*, A. Aziz*, X. Li, M. S. Kim, J. Sampson, S. Datta, **S. K. Gupta,** V. Narayanan, "Device –Circuit Co Design of FEFET Based Logic for Low Voltage Processors", *IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI)* 2016.

35) A. Aziz*, S. Ghosh, **S. K. Gupta,** and S. Datta, "Polarization Charge and Coercive Field Dependent Performance of Negative Capacitance FETs", *Device Research Conference (DRC)* 2016.

36) S. George*, K. Ma, A. Aziz*, X. Li, J. Sampson, A. Khan, S. Salahuddin, M.-F. Chang, S. Datta, **S. K. Gupta**, and V. Narayanan, "Nonvolatile Memory Design Based on Ferroelectric FETs", *Design Automation Conference (DAC)* 2016.

37) J. Frougier, N. Shukla, D. Deng, M. Jerry, A. Aziz*, L. Liu, G. Lavallee, T. S. Mayer, **S. K. Gupta** and S. Datta, "Phase-transition-FET Exhibiting Steep Switching Slope of 8mV/decade and 36% Enhanced ON Current", *IEEE Symposium on VLSI Technology*, 2016.

38) **S. K. Gupta,** A. Aziz*, N. Shukla and S. Datta, "On the Potential of Correlated Materials in the Design of Spin-Based Cross-Point Memories", to appear in *International Symposium on Circuits and Systems (ISCAS)* 2016 (Invited).

39) A. Aziz*, N. Shukla, S. Datta and **S. K Gupta**, "Implication of Hysteretic Selector Device on the Biasing Scheme of a Cross-point Memory Array", *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2015.

40) A. Aziz*, N. Shukla, S. Datta and **S. K Gupta**, "COAST: Correlated Material Assisted STT MRAMs for Optimized Read Operation", *International Symposium on Low Power Electronics and Design (ISLPED)*, 2015.

41) A. Aziz*, N. Shukla, S. Datta and **S. K Gupta**, "Read Optimized MRAM with Separate Read-Write Paths based on Concerted Operation of Magnetic Tunnel Junction with Correlated Material", *Device Research Conference (DRC)*, 2015.

42) A. Aziz*, W. Cane-Wissing*, M. S. Kim, S. Datta, V. Narayanan and **S. K. Gupta**, "Single-Ended and Differential MRAMs based on Spin Hall Effect: A Layout-Aware Design Perspective" *IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI)*, 2015 (Invited).

43) S. George*, A. Aziz*, X. Li, J. Sampson, S. Datta, **S. K. Gupta,** V. Narayanan, "NCFET Based Logic for Energy Harvesting Systems", *Semiconductor Research Corporation (SRC) TECHCON, 2015.*

44) M. S. Kim, W. Cane-Wissing*, J. Sampson, S. Datta, V. Narayanan and **S. K. Gupta**, "Comparing Energy, Area, Delay Tradeoffs in Going Vertical with CMOS and Asymmetric HTFETs" *IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI)*, 2015.

45) K. Ma, N. Chandramoorthy, X. Li, **S. K. Gupta**, J. Sampson, Y. Xie, V. Narayanan, "Using Multiple-Input NEMS for Parallel A/D Conversion and Image Processing", *IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI)*, 2015.

46) Xueqing Li, Unsuk Heo, Huichu Liu, **S. K. Gupta**, Suman Datta and Vijaykrishnan Narayanan, "A High-Efficiency Switched-Capacitance HTFET Charge Pump For Low-Input-Voltage Applications", *International Conference on VLSI Design*, 2015.

47) S. Datta, R. Pandey, A. Agrawal, **S. K. Gupta** and R. Arghavani, "Impact of Contact and Local Interconnect Scaling on Logic Performance", *IEEE Symposium on VLSI Technology* 2014. (Invited)

48) K. Ma, H. Lu, Y. Xiao, Y, Zheng, X. Li, **S. K. Gupta,** Y. Xie and V. Narayanan, "Independently-Controlled-Gate FinFET 6T SRAM Cell Design for Leakage Current Reduction and Enhanced Read Access Speed", "*IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI)*, 2014.

49) **S. K. Gupta,** W. Cho, A, Goud, K, Yogendra and K. Roy, "Design Space Exploration of FinFETs in sub-10nm Technologies for Energy-Efficient Near-Threshold Circuits", *Device Research Conference (DRC)*, 2013.

50) A. Goud, **S. K. Gupta,** S. H. Choday and K. Roy, "Atomistic Tight-Binding based Evaluation of Impact of Gate Underlap on Source to Drain Tunneling in 5 nm Gate Length Si FinFETs", *Device Research Conference (DRC)*, 2013.

51) **S. K. Gupta** and K. Roy, "Spacer Thickness Optimization for FinFET-based Logic and Memories: A Device-Circuit Co-design Approach", *Electro Chemical Society Symposium* 2012 (Invited) (**Rated amongst the top 8 papers in the conference**).

52) **S. K. Gupta**, J. P Kulkarni, S. Datta and K. Roy, "Dopant Straggle-Free Heterojunction Intra-band Tunneling (HIBT) FETs with Low Drain-induced Barrier Lowering/Thinning and Reduced Variation in OFF current", *Device Research Conference (DRC)*, 2012.

53) D. Lee, **S. K. Gupta** and K. Roy "High-Performance Low-Energy STT MRAM Based on Balanced Write Scheme", *International Symposium on Low Power Electronics and Design (ISLPED)*, 2012.

54) Y. Kim, **S. K. Gupta**, S. P. Park, G. Panagopoulos and K. Roy "Write-Optimized Reliable Design of STT MRAM" *International Symposium on Low Power Electronics and Design (ISLPED)*, 2012. (**Nominated for Best Paper Award**).

55) S. P. Park, **S. K. Gupta,** N. N. Mojumder, A. Raghunathan and K. Roy, " Future Cache Design using STT MRAMs for Improved Energy Efficiency: Devices, Circuits and Architecture", *Design Automation Conference (DAC),* 2012.

56) **S. K. Gupta**, S. P. Park, N. N. Mojumder and K. Roy, "Layout-Aware Optimization of STT MRAMs", *Design Automation and Test in Europe Conference (DATE)*, 2012.

57) **S. K. Gupta**, S. H. Choday and K. Roy, "Exploration of Device-Circuit Interactions in FinFET-based Memories for sub-15nm Technologies using a Mixed Mode Quantum

Simulation Framework: Atoms to Systems", *International Electron Device Meetings (IEDM)*, 2011.

58) X. Fong, **S. K. Gupta,** N. N. Mojumder, H. Choday, C. Augustine, and Kaushik Roy, "KNACK: A Hybrid Spin-Charge Mixed-Mode Simulator for Evaluating Different Genres of Spin-Transfer Torque MRAM Bit-cells", *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD),* 2011.

59) N. N. Mojumder**, S. K. Gupta** and K. Roy, "Dual Pillar Spin Transfer Torque MRAM with tilted magnetic anisotropy for fast and error-free switching and near-disturb-free read operations", *Device Research Conference (DRC)*, 2011.

60) S. Dighe, **S. K. Gupta**, V. De, S. Vangal, N. Borkar, S. Borkar and K. Roy, "A 45nm 48-core IA processor with Variation-Aware Scheduling and Optimal Core Mapping" *IEEE Symposium on VLSI Circuits*, 2011.

61) M. Sharad, **S. K. Gupta**, S. Raghunathan, P. Irazoqui, K. Roy, " Ultra Low Power, LPF-Only DWT Architecture for an Epileptic Seizure Prosthesis Implant", *Subthreshold Microelectronics Conference*, 2011.

62) K. Roy, J. P. Kulkarni and **S. K. Gupta**, "Device/Circuit Interactions at 22nm Technology Node", *Design Automation Conference (DAC)*, 2009 (Invited).

63) A. Goel, **S. K. Gupta,** A. Bansal, M.-H. Chiang and Kaushik Roy, "Double-Gate MOSFETs with Asymmetric Drain Underlap: A device-circuit co-design and optimization perspective for SRAM", *Device Research Conference (DRC)*, 2009.

64) S. Raghunathan, **S. K. Gupta**, H. Markandeya, K. Roy and P. Irazoqui, "Co-design of hardware and software to optimize seizure prediction and detection algorithms towards a closed loop epilepsy prosthesis", *Proceedings of the American Epilepsy Society(AES) Annual Meeting*, 2009.

65) S. Raghunathan, **S. K. Gupta**, K. Roy and P. Irazoqui, "An implantable ultra-low power digital circuit implementation of a seizure detection algorithm", *BMES Annual Fall Meeting*, 2009.

66) M. J. Kumar, V. Venkataraman and **S. K. Gupta**, "A New Grounded Lamination Gate (GLG) SOI MOSFET for Diminished Fringe Capacitance Effects," *Technical Proceedings of the 2006 NSTI Nanotechnology Conference and Trade Show,* pp. 709-712, 2006.

67) M. J. Kumar, V. Venkataraman and **S. K. Gupta**, "Compact Modeling of Parasitic Internal Fringe Capacitance and its effect on the Threshold Voltage of High-K Gate Dielectric SOI MOSFETs", *Int. Workshop on the Physics of Semiconductor Devices, 2005.*

Invited Talks

68) **S. K. Gupta,** "Energy Efficient and Non-Volatile Circuit Design based on

Ferroelectric Transistors", *Beyond-CMOS Circuits and Systems Workshop*, University of Notre Dame, 2016.

69) **S. K. Gupta,** "Low Power Robust Design of FinFET-based Circuits using a Technology-Circuit Co-optimization Approach", *9th International Front-End Electronics (FEE) Conference*, 2014.

Book Chapters (in chronological order)

70) **S. K. Gupta** and K. Roy, "Low Power Robust FinFET based SRAM Design in Scaled Technologies" *Circuit Design for Reliability*, 2015 (Ed. R. Reis, Yu Cao and G. Wirth), Springer New York.

71) V. Venkataraman, **S. K. Gupta** and M. J. Kumar, "Laser Processing of Materials in Nanotechnology," *Encyclopedia of Nanoscience and Nanotechnology*, 2nd Edition, 2008, (Ed. H.S.Nalwa), American Scientific Publishers, CA, USA.

72) X. Li, M. S. Kim, S. George*, A. Aziz*, M. Jerry, N. Shukla, J. Sampson, **S. K. Gupta**, S. Datta, and V. Narayanan, "Emerging Steep-Slope Devices and Circuits: Opportunities and Challenges", Submitted for possible publication in *Beyond CMOS*, 2017, Springer.

PATENT APPLICATIONS

1) **S. K. Gupta**, A. Aziz, N, Shukla, S. Datta, X. Li and V. Narayanan, "Correlated Material Enhanced Memories and Peripheral Circuits for Non-Volatile Storage" Application filed. (Application No: 62/346,207).

2) S. Raghunathan, **S. K. Gupta**, P. Irazoqui and K. Roy, "A Nano-power Real-time Seizure Detection System on Chip" Application filed. (Application No: 12/144.452).

3) M. J. Kumar, **S. K. Gupta** and V. Venkataraman, "A new grounded lamination gate structure for controlling parasitic fringe capacitance effects in MOSFETs," Application filed. (Application No: 1693/DEL/2006 dated 24-07-2006).

TEACHING

Penn State University

- Advanced Digital VLSI Design: EE597 *Spring 2017*
- Electronic Circuit Design 1: EE310 *Spring 2017*
- Digital Integrated Circuits: EE416/CMPEN416 *Fall 2016*
- Electronic Circuit Design 1: EE310 *Spring 2016*
- Digital Integrated Circuits: EE416/CMPEN416 *Fall 2015*
- Advanced Digital VLSI Design: EE597A *Spring 2015*
- Digital Integrated Circuits: EE416/CMPEN416 *Fall 2014*
- Design Tools : EE200 (With Prof. Jeff Schiano) *Spring 2014*

Purdue University

- Linear Circuit Analysis: ECE202 (as a graduate instructor) *Summer 2008*
- Electronic Design and Automation: ECE255 (as a teaching assistant) *Fall 2007*
- Electronic Design and Automation: ECE255 (as a teaching assistant) *Spring 2007*
- Electronic Design and Automation: ECE255 (as a teaching assistant) *Fall 2006*

SERVICE AND OUTREACH

Technical Program Committees in Conferences

- Chair of VLSI Circuits and Low Power Track, GLSVLSI (2017)
- Member of Technical Program Committee, DAC (2017)
- Member of Technical Program Committee, VLSIDAT (2017)
- Member of Technical Committee for DAC Ph.D. Forum (2016)
- Member of Technical Program Committee, GLSVLSI (2016)
- Member of Technical Program Committee, ISLPED (2015, 2016, 2017)
- Member of Technical Committee, IEEE S3S Conference (2014, 2015)
- Member of Technical Program Committee, VLSI India (2014)

Special Sessions in Conferences

- Organizer of special session on "Design Opportunities and Challenges in Non-Volatile Technologies" in ISQED (2017)
- Special session chair at Design Automation Conference (2015)
- Organizer of special session on Non-volatile Memories in ISVLSI (2015)

Service for Journals

- Reviewer: IEEE-TED, IEEE-EDL, IEEE-TCAS, IEEE-JETCAS, IEEE-TCAD, IEEE-TVLSI

Other Activities

- Hosted two students from under-represented groups under Summer Research Opportunity Program (2016)
- Participated in school outreach program, Exploration-U (2016)