



EE 210 Lab Exercise #5: OP-AMPS I



ITEMS REQUIRED	EE210 crate, DMM, EE210 parts kit, T-connector, 50Ω terminator, Breadboard
ASSIGNMENT	Lab report due at the beginning of the next lab period
Data and results from all of the numbered, bolded material in the procedure sections must be included and clearly numbered in the data section of the lab report.	

Introduction

The operational amplifier (op amp) was introduced in class for applications involving linear amplification. The op amp is an integrated circuit (IC) that contains over two dozen transistors and a dozen resistors as shown in Figure 1. However, by using the equivalent circuit model of the op amp, no background is needed in transistor amplifier analysis to design and build circuits using this device. In particular, the functionality of the op amp can be modeled using a simple combination of resistors coupled with a dependent voltage source as shown in Figure 2. Moreover, to analyze circuits that contain *ideal op amps*, the equivalent circuit model can be neglected and the golden rules that describe op amp behavior with negative feedback can be applied:

1. The voltage difference between the input is zero (valid if $A = \infty$).
2. The input terminals draw no current (valid if $R_{in}(\text{device}) = \infty$).

In the first two classes of this three-class lab, four op amp circuits that contain negative feedback are studied. These include the inverting, non-inverting, buffer, and summing amplifier configurations. In the third class, the open loop characteristics of the op amp will be explored, as well as its function as a comparator. Throughout the labs, the non-ideal characteristics of the op amp are emphasized. They are the saturation of the output voltage due to a limitation in the supply voltage and a limitation in the maximum output current of the op amp, and the finite frequency response of the op amp.

The Op amp Package

A LF412 dual op amp is used for all of the EE210 labs and projects. Data books are filled with hundreds of general and application specific op amps from IC manufacturers such as National Semiconductor and Texas Instruments. These data books are available in the EE stockroom and the EE 210 lab. Op amps come in sealed dual-in-line packages (DIPs). A top-view of the LF412 op amp DIP is shown in Figure 3 along with its pin-out. Figure 4 gives the circuit diagram and dc bias connections of this op amp. The circuit diagram indicates the need for both positive and negative dc bias voltages (power for the internal transistor circuitry). In this lab, $V_{CC} = +15\text{ V}$ and $-V_{EE} = -15\text{ V}$. The op amp will function properly with other supply voltages, however, for the LF412 the output will be limited to approximately $V_{CC} - 1\text{ V}$ and $-V_{EE} + 1\text{ V}$. Using $\pm 15\text{ V}$, this means that the maximum output will be limited to $\pm 14\text{ V}$. Bypass capacitors (you will learn the theory behind these later in EE 210) are included in Figure 4 between the supply pins and ground to eliminate high frequency noise that is common in many circuits. Periodically throughout the lab, remove the bypass capacitors and watch for noise on the output signal. Noise is not part of the theory, but it is part of real world circuit design!

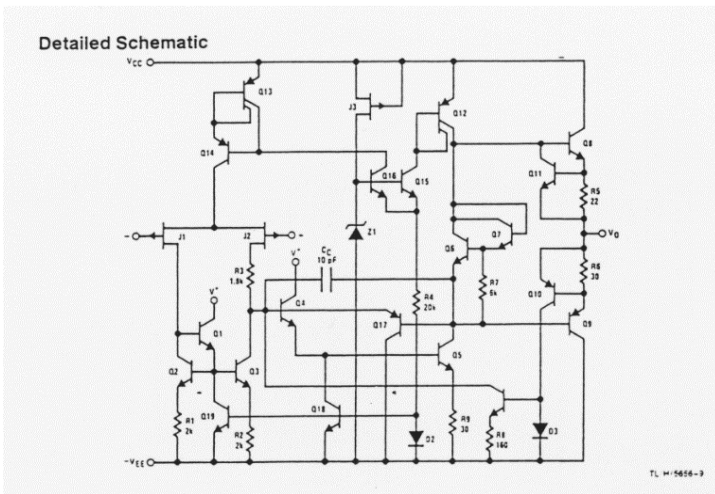


Figure 1: Integrated circuit schematic for the National Semiconductor LF412 op amp.

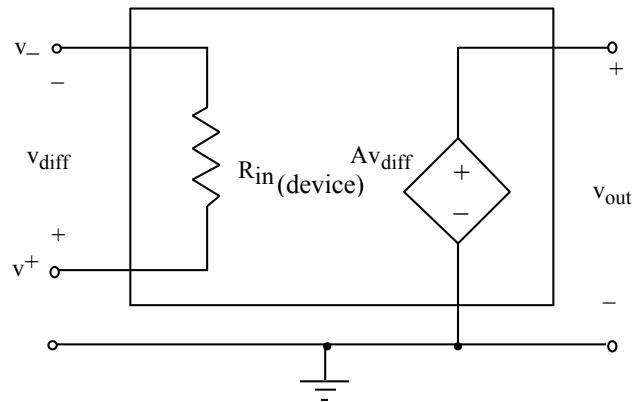


Figure 2: Equivalent circuit model of the op amp. For most op amps, $R_{in}(\text{device})$ is approximately $10\text{ M}\Omega$ and A is approximately $100,000\text{ V/V}$ (at low frequencies). The ideal op amp assumes $R_{in}(\text{device}) = \infty$ and $A = \infty$ (simplifies circuit analysis while providing good accuracy).

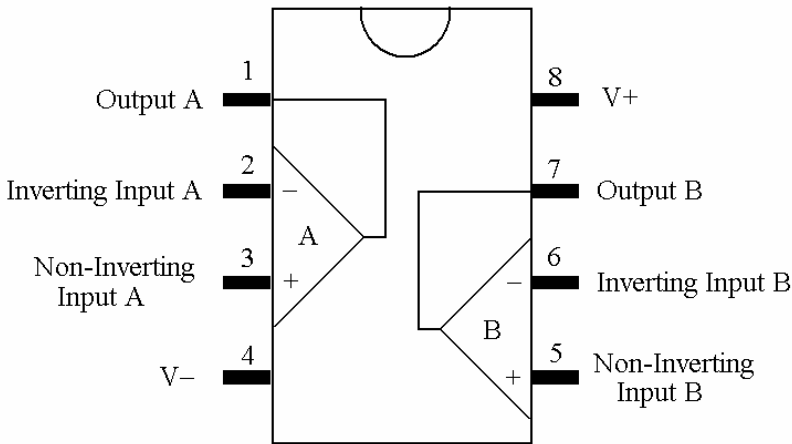


Figure 3: Dual-in-line package (DIP) along with the pin-out of the LF412 dual op amp.

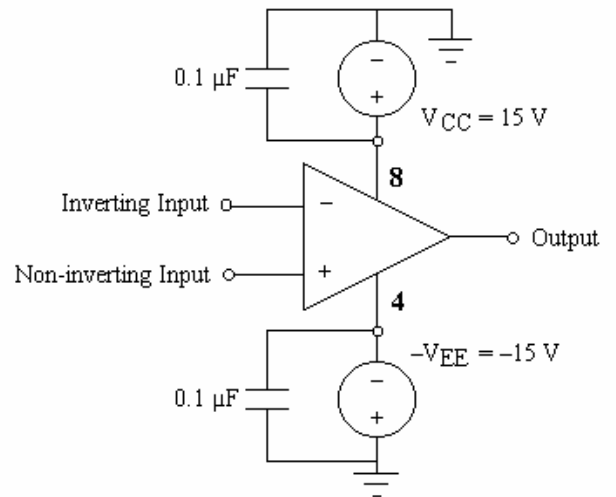
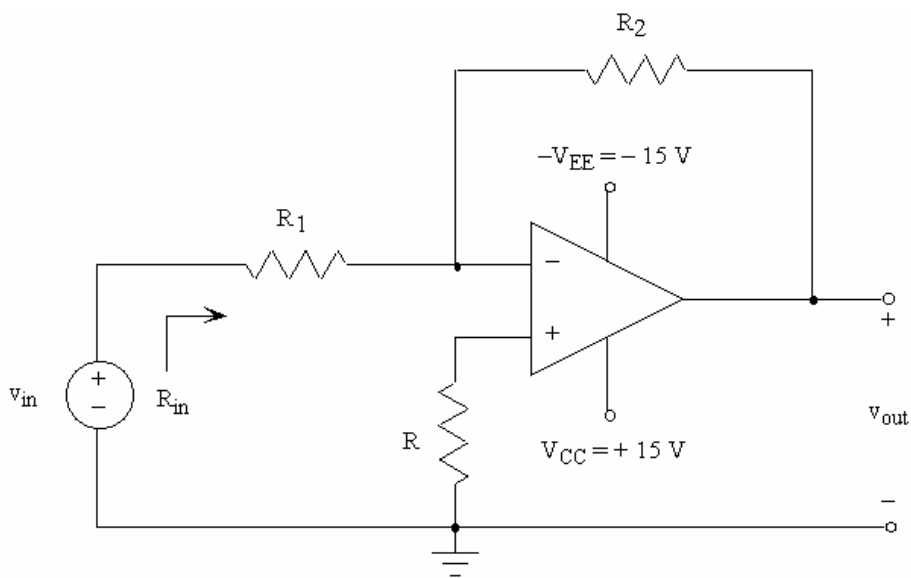


Figure 4: Circuit diagram for an op amp including dc power connections. The bypass capacitors are included to reduce the noise that is present in the circuit.

Exercise 1: The Inverting Voltage Amplifier

In this exercise, the op amp circuit is arranged negative feedback configuration. In other words, the output is coupled back to the input in such a way that part of the input is canceled. At the expense of reducing the gain, negative feedback improves the linearity, frequency response, noise performance, and stability of the amplifier. As will be seen after completing the third op amp lab, with negative feedback, the characteristics of the amplifier circuit do not depend on the open-loop characteristics of the op amp, but instead depend on the properties of the feedback network.

The first closed-loop (negative feedback) configuration that is studied is the inverting configuration shown in Figure 5. In this configuration, the voltage gain v_{out}/v_{in} is determined by the ratio of the resistors R_1 and R_2 . This configuration amplifies and inverts the output voltage waveform relative to the input voltage waveform.



Note: Theoretically, R is not needed. It can be included to reduce the effects of a finite input bias current.

$$v_{out} = -(R_2/R_1)v_{in} \quad \text{-- for ideal op amp}$$

Figure 5: Closed-loop inverting op amp configuration.

Part 1: DC Input

Part 1: Procedure

1. Using the values of R_1 and gain given for the inverting configuration in the *pre-lab* exercise, **(1) include the calculations of R_2 and determine the maximum input voltage signal that can be applied to the amplifier before the output becomes distorted (output clips at $\pm 14\text{ V}$).**
2. Using an LF412 op amp, construct the closed-loop inverting op amp circuit shown in Figure 5. Adjust the +6V terminal on the dc power supply to the dc value of V_{in} given in part 1c(i) of the *pre-lab* exercise.

- Using the DMM, (2) measure the open circuit output voltage. (3) Determine the experimental gain.
- Using the DMM, (4) measure the current flowing from the source. (5) Determine the experimental input resistance R_{in} (see Appendix) of the *amplifier configuration* (not the device), including the theoretical calculation of R_{in} from the *pre-lab exercise*. (6) Also, measure the voltage at and the current into both the inverting and non-inverting terminals.
Note: When determining R_{in} for this configuration, consider the virtual ground at the inverting input.
- Vary the dc input voltage between 0 to +6V. (7) Make a sketch of V_{out} vs. V_{in} , noting the slope of the linear portion of the plot.

Part 2: Sinusoidal Input

Part 2: Procedure

- Disconnect V_{in} from the +6V terminal of the dc power supply.
- Configure the waveform generator to the sinusoidal value of V_{in} given in part 1c(ii) of the *pre-lab* exercise and use this signal as the input to the op-amp (V_{in}).
- Monitor simultaneously the input (across the waveform generator) of the circuit using CH 1 of the oscilloscope and the output (between the output node of the op amp and ground) of the circuit using CH 2 the oscilloscope. Both waveforms must be displayed simultaneously to provide information regarding the phase shift between the input and the output voltage waveforms. (8) **Print both waveforms including V_{p-p} of the input and output voltage waveforms.** (9) **Determine the phase shift between the input and output voltage waveforms.** (10) **From the input/output plots, determine the measured closed-loop voltage gain.**
- Vary the sinusoidal input voltage and observe the output waveform. (11) **Comment on the value of the closed-loop voltage gain as a function of input voltage.** (12) **Determine the minimum value of the input voltage that saturates (results in clipping of) the output.**
- Vary the dc offset of the input voltage and observe the output waveform. (13) **Determine the relationship between the offset of the input and the offset of the output when the output is not clipped.**
- With a peak-to-peak input voltage of 2V peak to peak, (14) **Record the values of the closed-loop voltage gain for 100, 1k, 10k, 100k, 300k, 500k, 1M, 5M (Hz) and create a plot (use logarithmic spacing on the frequency axis).** (15) **Note what happens to the phase shift as the frequency is increased and record the intermediate frequency where the gain begins to drop significantly.**

Exercise 2: The Non-Inverting Voltage Amplifier

The second closed-loop (negative feedback) configuration that is studied is the non-inverting configuration shown in Figure 6. In this case, the voltage gain v_{out}/v_{in} is equal to $1 + R_2/R_1$.

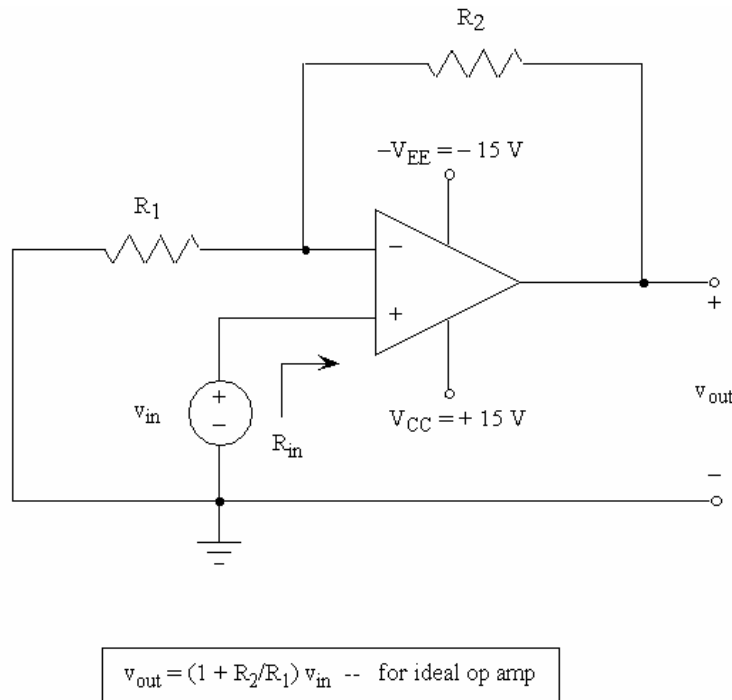


Figure 6: Closed-loop non-inverting op amp configuration.

Part 1: DC Input

Part 1: Procedure

1. Using the values of R_1 and gain given for the non-inverting configuration in the *pre-lab* exercise, **(16) include the calculations of R_2 and determine the maximum input voltage signal that can be applied to the amplifier before the output becomes distorted (output clips at ± 14 V).**
2. Using an LF412 op amp, construct the closed-loop inverting op amp circuit shown in Figure 6. Adjust the +6V terminal on the dc power supply to the dc value of V_{in} given in part 2c(i) of the *pre-lab* exercise.
3. Using the DMM, **(17) measure the open circuit output voltage. (18) Determine the experimental gain.**
4. Using the DMM, **(19) measure the current flowing from the source. (20) Determine the experimental input resistance R_{in} (see Appendix) of the *amplifier configuration* (not the device), including the theoretical calculation of R_{in} from the *pre-lab* exercise. (21) Also, measure the voltage at and the current into both the inverting and non-inverting terminals.**
6. Vary the dc input voltage between 0 to +6V. **(22) Make a sketch of V_{out} vs. V_{in} , noting the slope of the linear portion of the plot.**

5. Part 2: Sinusoidal Input

Part 2: Procedure

1. Disconnect V_{in} from the +6V terminal of the dc power supply.
7. Configure the waveform generator to the sinusoidal value of V_{in} given in part 2c(ii) of the *pre-lab* exercise and use this signal as the input to the op-amp (V_{in}).
2. Monitor simultaneously the input (across the waveform generator) of the circuit using CH 1 of the oscilloscope and the output (between the output node of the op amp and ground) of the circuit using CH 2 the oscilloscope. Both waveforms must be displayed simultaneously to provide information regarding the phase shift between the input and the output voltage waveforms. **(23) Print both waveforms including V_{p-p} of the input and output voltage waveforms (24) Determine phase shift between the input and output voltage waveforms. (25) From the input/output plots, determine the measured closed-loop voltage gain.**
3. Vary the sinusoidal input voltage and observe the output waveform. **(26) Comment on the value of the closed-loop voltage gain as a function of input voltage. (27) Determine the minimum value of the input voltage that saturates (results in clipping of) the output.**
4. Vary the dc offset of the input voltage and observe the output waveform. **(28) Determine the relationship between the offset of the input and the offset of the output when the output is not clipped.**
5. With a peak-to-peak input voltage of 2V peak to peak, **(29) Record the values of the closed-loop voltage gain for 100, 1k, 10k, 100k, 300k, 500k, 1M, 5M (Hz) and create a plot (use logarithmic spacing on the frequency axis). (30) Note what happens to the phase shift as the frequency is increased and record the intermediate frequency where the gain begins to drop significantly.**

Appendix: Input Resistance of a Circuit

The equation for calculating input resistance is: $R_{in} = V_{in} / I_{in}$, where V_{in} is the input voltage and I_{in} is the current flowing into the circuit (with some equivalent resistance) from the source or previous stage. See Figure 9 below. This can be used to determine the input resistance of any type of known or unknown ("black box") circuit; it is not limited to op-amp circuits.

Input resistance is important because a circuit with a finite input resistance acts as a load (see Lab #4), and this must be taken into consideration when designing circuits such as cascaded circuits (Lab #6).

Note: The input resistance (R_{in}) of a given op-amp circuit configuration may not equal the internal input resistance ($R_{in(device)}$) of the op-amp!!!

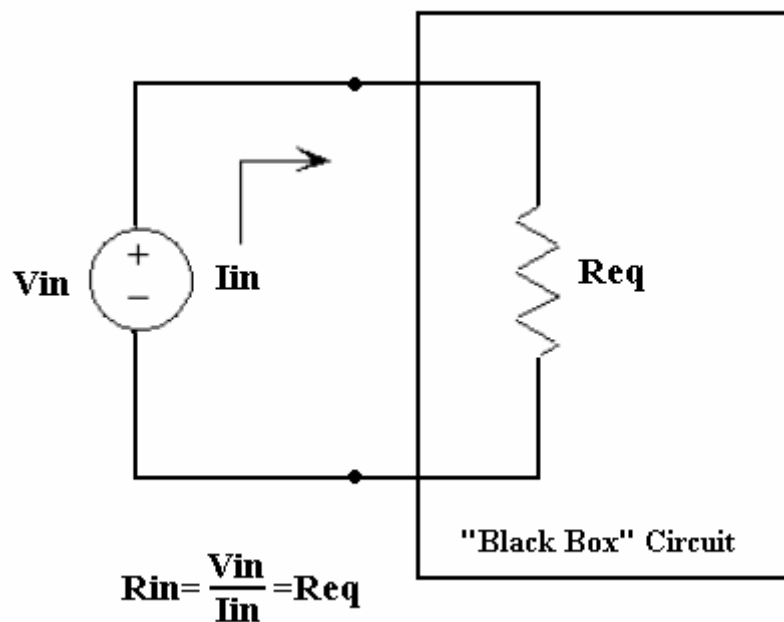


Figure 9: Input resistance of an arbitrary known or unknown ("black box") circuit with some equivalent resistance (R_{eq}).

Discussion Questions

Discuss and thoroughly explain each of numbered the concepts below, listed by exercise. When applicable, consider the following items when formulating your responses:

- A comparison of theoretical and experimental results.
- An identification and description of the likely sources of error.
- A description of the purpose and function of each circuit and possible applications.
- A comparison of similar circuits in the lab and the respective functions.
- A discussion of relevant observations, results, and deductions.

Exercises 1 & 2

1. Discuss and compare the significance of the various properties and limitations of each configuration including, gain, phase shift, input resistance, and the frequency response.
2. Compare the analytical values to the experimental values and the results from the *pre-lab* exercises. Explain any discrepancies and discuss the possible sources of error.
3. Discuss the significance of input resistance. Does it relate to any concerns introduced in Lab #4
4. Which configuration would load a source? Why?
5. Discuss and compare the gain plots of each configuration. What are the similarities and differences between the plots?
6. Discuss and compare the frequency response plots of each configuration. What are the similarities and differences between the plots?
7. How does each amplifier respond to the DC offset of an AC input signal? Are these responses the same as each amplifier's response to a pure DC input signal?
8. Does the input resistance of an amplifier change if the input is AC or purely DC? Explain.
9. Compare the results of Exercise 1 and 2, drawing some conclusions about the two configurations and closed loop configurations in general. In what situations would each configuration be more appropriate.